

<b>Notice of References Cited</b>	Application/Control No. 10/731,566	Applicant(s)/Patent Under Reexamination VANDLING, GILBERT C.	
	Examiner Vuthe Siek	Art Unit 2825	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
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**FOREIGN PATENT DOCUMENTS**

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**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Girard et al., "A Trace-Based Method for Delay Fault Diagnosis in Synchronous Sequential Circuits," IEEE, 1995, pages 526-532.
	V	Ranjan et al., "Using Combinational Verification for Sequential Circuits," IEEE, Jan 1999, pp. 1-7.
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
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